Wide-Band Packet Radio Technology

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Invited Paper

Advances in signal processing and architectural design for highperformance packet radio are described. The scope of the work roughly encompasses the data-link and physical levels of standardized layered-network architectures. A hardware-function layering approach is used, including the purposeful design of an interface to provide a structured control environment for a demonstration packet radio. The advanced signal processing provides a robust, flexible data link to service demanding network environments, and uses 100-MHz-bandwidth surface-acoustic-wave (SAW) convolvers as large time-bandwidth product matched filters for communication with nonrepeating pseudonoise waveforms. The convolvers are combined with a binary-quantized postprocessor to implement a hybrid correlator which provides high processing gain for detection, demodulation, and ranging measurements. Data rates can be selected, in response to varying channel conditions, over a range from 1.45 Mbits/s down to 44 bits/s with an almost ideal tradeoff in processing gain for interference rejection and privacy ranging from 18 dB up to 61 dB. Future enhancements are proposed that will advance both the signal processing and the architecture.

I. INTRODUCTION

The general objective of advanced packet radio technology is to make more efficient use of and to offer greater protection to network resources. While the network- and higher protocol-level technologists are developing network architectures, routing, and control strategies [1], [2], the data-link- and physical-protocol-level technologists are developing new signal processing concepts, devices, and circuit architectures to create robust links to service the network [3]. As will become clear throughout this paper, it is essential that these two groups of designers become much more closely coupled in order to exploit the maximum capabilities of each effort.

This paper describes major advances in the data-link and physical layer technologies and elucidates several potential

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growth areas. A demonstration radio has been built which exploits advanced signal processing based on surfaceacoustic-wave (SAW) devices [4] for high-performance, near-100-MHz-bandwidth pseudonoise (PN) spread-spectrum communication [5] at data rates as high as 1.45 Mbits/s. In building a radio with this advanced technology, it was appropriate to adopt an advanced architecture which could exploit the capabilities offered by the technology and also meet the need for sophisticated network operation. We will describe the radio architecture in the first section of the paper and the structure and functions of the signal processor used in the radio in the second section. We will also describe the impact of the signal processing on the network. The goal of the demonstration radio was to achieve the realizable limits of wide-band packet radio performance using the most advanced, practical technology available, while also maintaining a credible package size. (Fig. 1 shows a photograph of the radio.) As an outgrowth of the



Fig. 1. Photograph of the radio hardware. The *L*-band RF unit is on the right. The other three units reside in the chassis on the left.

radio design, several as-yet-unexplored problem areas regarding both the signal processing and the interface to the network-level protocols have been identified. The fourth section of the paper enumerates enhancements that could alleviate these problem areas. Various aspects of the signal processing and protocol design have been described in finer detail in other papers [6]-[8].

This radio can be contrasted with the Low-Cost Packet

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Radio (LPR) also described in this issue. The intention of the LPR is to proliferate a large number of modest-performance (12.5-MHz spreading bandwidth) radios. In keeping with its goal, the demonstration radio we describe offers nearly an order of magnitude more bandwidth, up to 40 dB more processing gain, and a wide range of functions which support robust network data links.

Broadcast-network radio environments pose great difficulties because they compound all the communication channel problems of point-to-point radios with the mutualinterference and connectivity-control problems of multiple nodes. Problems in the channel may take several forms. Interference, whether intentional or not, is likely to be present. There may also be a requirement to avoid undesired detection or eavesdropping. Additionally, there can be multiple reflections of the transmitted signal of varying amplitude and phase (multipath) in a ground communication environment. Any reaction to these problems taken in isolation from comprehensive network considerations may have further negative impacts.

Networks operating with mobile nodes must function in rapidly changing environments, and even fixed networks often experience a time-varying channel. In the past, many packet radio networks have been designed so that response to problems occurred only at the network level. Nodes were switched out and the offered traffic was alternately routed. This scheme applies for node hardware failures as well as problems in the communication channel. However, alternate routing causes congestion in other areas of the network, and, if the interference is changing, the network must continually react with corrective routing. Alternatives to this approach must be made available at the data-link and physical levels. For high performance, the radio is required to measure the channel and adapt the signalprocessing and the radio-operating parameters, such as the transmit data rate, to the changing conditions. The network level looks upon the radio nodes as dynamically allocatable resources; each radio node must treat its signal-processing capabilities analogously.

In Fig. 2, a simple network connection is drawn to illustrate this behavior. The packets are to be routed between computers *A* and *B*. In this example, an outside transmitter interferes with the repeater labeled *R* and, as a result, the network control software alternately routes the packets as



Fig. 2. A simplified packet-radio network scenario with communications between computers A and B by way of repeater R. An interference source causes errors and lost packets. A robust data link is required to overcome the interference.

shown by the dashed lines. A simple protocol might be to alternately route if 60 percent of the packets were not successfully received in communications with node R [9]. Alternatively, if the radios have the adaptive signal processing described herein, instead of avoiding that connection they could burn through the interference by increasing the transmit power, or add further processing gain by lowering the data rate, or use a combination of both techniques. Increasing the transmit power decreases privacy as well as affecting the net connectivity; thus this parameter may not be an available degree of freedom in many scenarios. Of course, lowering the data rate reduces the instantaneous throughput, although the reduction in errors may allow a higher percentage of successful packets and possibly a net increase in throughput. The ability to trade reduced data rate for increased processing gain provides a "graceful degradation" of link quality rather than the abrupt removal of the link from the net. Another method that will be reviewed is the use of adaptive interference cancelers. Inherent in the implementation of the adaptive circuits are some channel measurements which are useful at the network level in deciding how best to apply the signal-processing assets. The impact at the network level is that the protocol for controlling the radios becomes substantially more complex, and a number of parameters are added to the distributed control algorithms of the network.

The past decade has brought the refinement of wide-band SAW convolvers [10] coupled with innovative signal processing techniques for direct-sequence spread-spectrum packet radio. A digital processor using an efficient butterfly algorithm to perform, via fast Fourier transforms, convolution equivalent to that of the highest performance convolvers available would have to run at about 10¹¹ fixed-point arithmetic operations per second (ops) [11]. In current digital technology, this level of performance would require thousands of dedicated large-scale integrated circuits and kilowatts of power. Alternatively, SAW convolvers are passive components that operate with just a few watts of RF amplification. Furthermore, SAW technology is physically robust and has been used in the rugged conditions of mobile and satellite applications.

There are many advantages to PN direct-sequence spreadspectrum modulation. The advantages arise because the signal is instantaneously spread in bandwidth, giving protection against interference, interception, and multipath. One criticism unjustly aimed at PN waveforms is that they require lengthy synchronization times. PN code acquisition, as it is called, is a topic of great interest in the design of serial-correlator receivers [12]. As will be explained in the signal processing section, convolvers behave as matched filters which operate completely asynchronously to the RF phase and code timing. Another criticism concerns the code division multiple access behavior of the PN system. The cross-correlation sidelobes of multiple-access PN waveforms may require suppression by more than the available processing gain. Nonlinear cancellation techniques which are not included in the present radio but which show promise in solving this problem are reviewed in the final section.

Within the paper, a number of features are described that provide robust communications. For interference suppression in the current radio we use large time-bandwidth waveforms with nonrepeating spreading codes, fast automatic-gain-control (AGC), and constant-false-alarm-rate (CFAR) circuitry [13]. The use of PN-coded spreading waveforms, transmit-power control, and ultrahigh processinggain modes facilitate private communication. For antimultipath processing we use RAKE demodulation [14]–[16] which accumulates the multipath energy for a single data bit (the energy is literally "raked" up), special multipathprecursor detection circuits for performing accurate ranging, nonrepeating spreading codes which suppress intersymbol interference, and multipath-resistant CFAR. To aid in the networking tasks, the radio is equipped for special packet types and is able to nearly optimally trade processing gain for data rate. Also, receiver-threshold control is used as a dual to transmit-power control.

The last section on enhancements and future directions discusses several areas of current work: new device technology, adaptive interference cancellation, and the data-link control software. The first two will offer the network further advances in robust signal processing technology while the third issue is of paramount importance for the network to make use of the flexibility offered by the signal processing. It is important to recognize that the signal-processing power of the SAW convolvers stems from the simultaneous capabilities of long interaction time and wide processing bandwidth. In the past, charged-coupled devices (CCDs) which offer long interaction times have been used at much lower bandwidths. Now CCDs are rapidly advancing to bandwidths that are commensurate with modest bandwidth packet radio at a fraction of the size and cost of the current SAW devices, [17]. A brief review of this advancing technology will be made. We will also review recent developments in signal excision and cancellation techniques which allow the RF front end to adapt to the changing network environment. When the linear processing described in the demonstration radio is insufficient at the required data rates, interference cancelers may be used. Finally, as previously mentioned, the interface between the distributed network-level control algorithms and the data-link capabilities is not well understood. This problem will inhibit the application of the most advanced technologies to packet radio. This discussion concludes with a proposal for the future directions in the approach of this problem.

11. THE DEMONSTRATION PACKET RADIO ARCHITECTURE

Hardware

Fig. 3 shows a block diagram of the radio, which consists of an RF unit, a modem, an error control unit (ECU), and a microcomputer. The RF unit performs the frequency translation between the IF and RF bands and contains the AGC, transmit power control, and amplifiers. The modem exploits advanced SAW-based technology combined with digital postprocessing to provide multifunction spreadspectrum signal processing. It performs the modulation and demodulation between the baseband data at the ECU and the IF waveform at the RF unit. The ECU employs advanced and versatile error-correction techniques for encoding and decoding between the baseband data at the microcomputer and the modem. The microcomputer runs network protocols, packetizes the messages, and initiates the local radio activity.

During transmit, a packet will be sent from the microcomputer to the ECU to be encoded, then to the modem where a data-link-level header is attached and the packet



Fig. 3. Block diagram of the radio with the control interface on the left and the data interface on the right for the modem, ECU, and the microcomputer. The controls for the RF unit are multiplexed onto the LO line.

is modulated onto the IF band, then to the RF unit where it is upconverted to the carrier frequency and transmitted. During receive, the process is reversed. The data-link header, which describes the modulation, coding, and packet parameters, is removed and examined in the modem. Fig. 1 shows the entire radio hardware. The RF unit is in the separate chassis on the right. The modem, ECU, and microcomputer are in the chassis on the left.

RF Unit

The RF unit converts between the 300-MHz IF and the 1.8-GHz (*L*-band) RF frequency. This RF band has been used extensively for DARPA's experimental packet radios and hence is used here. The receiver and transmitter share a common antenna and are isolated by a circulator. The front end is half duplex. The transmitter power is selectable over a 20-dB range, in 5-dB steps up to 15 W maximum, under control from the modem. During receive the AGC provides a virtually constant +10-dBm output to the modem for an input signal range of -80 to 0 dBm. The error voltage of the AGC feedback loop is continuously measured and sent to the modem as an observable parameter, reflecting the level of received power.

Modem

The modem unit comprises analog and digital signal-processing circuits and control logic. SAW convolvers provide programmable matched filtering with 33-dB processing gain (instantaneous time-bandwidth product of 2000). The SAW devices are coupled with digital postprocessing for detection, demodulation, and ranging measurements. A hybridcorrelator technique has been devised to extend the convolver processing gain to as much as 61 dB over a wide processing window. This hybrid analog/digital approach uti-

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Mode No.	Code Acquisition	TOA Measurement	Data	Function
1	Matched filter mode*	time stamp only	1.45 Mbits/s	least robust highest throughput
2	Matched filter mode*	time stamp with incoherent correlator correction	90.9 kbits/s	nominally robust nominal throughput improved ranging measurements
3	Matched filter mode*	time stamp only	90.9 × 2 [−] * kbits/s	fast synchronization private communication
4	Matched filter mode*	time stamp with coherent correlator correction	none	best ranging measurements
5	Correlatet	time stamp only	90.9 × 2 ⁻ * kbits/s	ultra robust lower throughput

*Burst synchronization using 11-µs symbols (7 sync, 9 verify, 18 header).

+Correlation synchronization using single symbol (11×2^{N} -µs symbol, 2.7-µs search window).

‡2 ≤ *N* ≤ 11.

lizes a convolver matched filter and a binary-quantized integrator. The binary integrator accumulates many successive matched-filter outputs on a sample-bin-by-samplebin basis to extend the 33-dB processing gain provided by the convolver [13]. The data rate can be selected, in response to varying communication channel conditions within the network, from 1.45 Mbits/s down to 44 bits/s with an almost ideal tradeoff in processing gain. Each factor of two in data rate results in a ~3-dB increase in signal-to-noise ratio at the output of the processor. All data rates use the full spreading bandwidth but different bit durations and hence time-bandwidth products. While the lowest data rates may not provide sufficient throughput in most circumstances, small but critical messages can be sent with a maximum robustness.

The modem uses the hybrid signal processor in a multitude of configurations (Table 1) which are application-dependent and are determined by the network-level commands that are sent to the control logic. First there is PN code acquisition; the initial detection of a signal, and the synchronization of the receiver's timing to that of the transmitter. As seen in Table 1, code acquisition may occur in either the asynchronous matched-filter mode, in which case the arrival time of the message need not be estimated, or the hybrid-correlator mode, which has superior processing gain but requires a prior estimate of the arrival time (to within 2.7 µs). If the matched filter is used for code acquisition, either the matched filter or the correlator may be used for demodulation. If the correlator is used for code acquisition, it is also used for demodulation. Matched-filter code acquisition occurs in the first 77 μ s after the signal reaches the receiver. Then the detection is verified to prevent excessive receiver blanking due to false alarms. The data-link header is demodulated to determine what type of packet it is, what the data rate is, and how long the packet is. Describing the demodulation characteristics in the datalink header allows the flexibility of a variety of packet parameters without burdening the network level with the excessive overhead required by prenegotiation of the parameters by the radio nodes. If detection in the hybrid correlator mode is required, the prenegotiation at the network level of the approximate arrival time of the signal implies that the demodulation characteristics such as data rate, length, and coding can be also readily preset.

The time of arrival (TOA) of the signal is initially determined during code acquisition in the matched-filter mode and can be improved using the hybrid correlator. The TOA combined with the time of transmit that is marked in the network-level header provide the network with information regarding clock offsets between radios and inter-radio range measurements which support self-location network algorithms. The range is measured to approximately 3-m resolution. In non-line-of-sight propagation conditions, the hybrid correlator can provide an improved TOA estimate by integrating the weak, direct-path signal to detectable levels.

The matched filter coherently demodulates at either 1.45 Mbits/s (Table 1, Mode 1) or 90 kbits/s (Mode 2) depending on the processing gain required. During Mode 2, the binary integrator noncoherently operates on the data stream to provide a TOA correction. If additional processing gain is needed for data demodulation (Mode 3), the binary integrator is used in either coherent or noncoherent operation from 22.7 kbits/s down to 44 bits/s by factors of two depending on the network requirements and electromagnetic environment. The multipath is noncoherently accumulated during demodulation at all data rates. As the binary integrator is used for data demodulation in Mode 3, it does not offer the TOA correction capability of Mode 2. Alternatively, a control packet can be invoked that uses the higher gain coherent processing for TOA after matched filter acquisition; however, no data can be contained in this type of packet (Mode 4).

The detailed structure of the hybrid signal processor will be discussed further in the signal processing section.

Error Control Unit

Sophisticated, flexible, forward error correction is used to further enhance the robustness of the packet radio. The ECU serially encodes and decodes digital data for error detection and correction. On transmit, it appends a 16-bit cyclic-redundance-check (CRC) word to the data received from the microcomputer, convolutionally encodes the data [18], scrambles the data in 256-bit blocks (for burst-error immunity), and then passes the result to the modem. On receive, the ECU unscrambles the data from the modem, decodes it using a sequential decoding algorithm, checks the CRC word for any errors previously undetected, and then passes the corrected data to the microcomputer. A variety of coding levels are available, selected according to desired performance and the coding overhead that can be afforded. The ECU determines the actual length of the packet, which is a function of the coding used. The upper limit on packet length is 8 kbits. The encoder/decoder section uses a dedicated VLSI chip [19] to perform error correction at the full 1.45 Mbits/s required.

Microcomputer

The microcomputer is a two-channel, direct-memory-access controller associated with a 68000-based general-purpose processor. The microcomputer may perform higher level control functions for the radio, particularly the network-level functions. The data-link-level radio functions are supervised by the microcomputer through the transfer of a set of control information each 10 ms. The microcomputer interfaces to the radio through special-purpose serial interface hardware and interfaces to a host computer through either a shared memory or an Ethernet connection. Packet transmit times are noted in the transmitted packet networklevel header and the receiver measures the arrival time. These data are used to calculate time-of-day offsets between radios for global time-of-day negotiation and range between radios in the network used by the distributed network-control algorithms to determine the relative location of all the radios in the network.

Interface

Control information and transmit and receive data for the ECU, modem, and microcomputer are passed between units by point-to-point, serial, simplex connections with asynchronous flow control (Fig. 3). Since it is often desirable to have the RF unit operate in a physically remote site from the rest of the radio, the control signals for the RF unit are multiplexed onto the local oscillator cable to minimize the interconnects. Each transmit and receive data interface between units consists of two of the simplex connections to form a full duplex link. The interface is intended to create a "loose" coupling between the units, thus creating structured layers.

Layering

Computer science in general and communication networking in particular have benefited greatly from incorporating layering into the design of large systems. The system is stratified into significant subunits or layers that form a hierarchy. Each layer utilizes the services of the layer directly below it and provides services to the layer directly above it in the hierarchy. The most apparent result of layering is the division of the design problem into manageable segments with specifiable interfaces. The layers are designed to work within a system-wide architectural standard; however, the details of the implementation of each layer are, in concept, independent of each other. Another advantage is that after spending many man-years designing a large system, an individual layer may be improved without affecting the rest of the system. Although layering has primarily been applied to software design, it is of extreme importance in the design of modern radio communications systems which are highly complex, are based on rapidly changing technology, and are themselves heavily softwarebased. Furthermore, the potential complexity of activity and control of the physical-, the data-link-, and the lower level network layers that results from advanced adaptive signal processing techniques and algorithms, requires that sophisticated management protocol like that invoked in the higher levels of software also be applied at these lower levels.

Often, a great deal of attention is paid to managing the software organization in packet-radio network design. Commensurate attention must be paid to managing the advanced-technology hardware; otherwise, the result can be a tightly woven web of interface lines tying together seemingly unstructured subunits. The approach should be to hierarchically segment the radio structure from the beginning of a design with a well-defined interface which loosely couples the segments or layers. As the design progresses, every effort is then made to retain the structure, with the rationale that the overhead to do so is well worth the result. As a rough estimate, the overhead due to layering in this radio is around 10 percent of the hardware. Yet, each unit was designed by a different team of people and, after several successful retrofit designs, the structure and interface remain intact.

The layering in this radio is parallel to network-protocol layering [2], [20], [21]; however, there is not a one-for-one correspondence. We have chosen to layer our radio into the units shown in Fig. 3, with the RF unit on the lowest tier in the hierarchy. One could attempt to fit these units into the widely accepted models of the network, data-link, and physical layers [22], [23]. However, these conventions can be ambiguous and inappropriate when applied to advanced signal-processing techniques. Some signal-processing functions which only make sense when used at the front end (the point closest to the medium) have a direct effect on the attributes of what is typically considered the data link domain. Thus the two layers tend to become merged. Although the layering concept works well, the resulting defined structure can lose its validity if applied too generally.

Time Frame

It is necessary to identify the time scales in which the layers operate in order to approach a minimal yet flexible interface design. Network fluctuations are assumed to occur on a time scale that is of the order of tens of seconds to hours. The microcomputer must react to these network fluctuations to support the control of the network dynamics. Similarly, the microcomputer must control the other units of the radio on a much finer time scale than that on which it reacts. Thus the radio-control time scale is divided into 10-ms control time slots that allow the microcomputer to read the radio status, change parameters, and generate activity in the radio. The network uses these time slots to change spreading code seeds (PN start vector), control contention, and align global time of day between radios. The modem must react to the control-time-slot activity and consequently implement radio utilities and perform packet communication with much finer resolution. Examples of radio utilities are data-link connectivity control, time-of-day alignment, and transmit-receive prioritization.

To illustrate the relationship between the four units in the architecture, we discuss the activity of a radio as it receives a packet. The radio idles awaiting a reception. The arrival time of a received packet is random and asynchronous. The RF unit and the modem are active in order to acquire a new signal; the ECU remains inactive; the microprocessor may be active in running a network protocol algorithm, but is unconcerned with the signal-processing activity at this time. This state is maintained until a packet detection occurs in the signal-processing circuits. Only the modem is cognizant that a valid pocket is being received, so it has the responsibility of awakening the ECU to begin decoding the demodulated data. The microprocessor becomes involved when the received packet is transferred from the ECU.

The transmitting radio indicates the packet parameters to the receiver with the data-link header. The receive modem demodulates the header and passes the code rate and length of the message to the ECU as its control information. Since the ECU as a layer must be transparent to the modem in the way it does its decoding, only the ECU can translate between the actual number of information data bits and the number of transmitted channel bits. Thus the ECU layer must indicate actual packet length to the modem. Since the microcomputer of the transmit radio node makes the coding and length decisions, the modem is actually carrying out orders of a layer higher than the ECU within the network in awakening and sending control information to the ECU.

Thus the interface requires three sets of control-related information to be transferred between the layers; commands, status, and observations. Command instructions come from the microcomputer level and go to the modem. The modem then redirects packet-specific command information to the RF unit and the ECU. As dictated by the layering hierarchy, the modem may only pass to the ECU commands issued from a microcomputer (possibly any one at the microcomputer peer level in the network) at the time and under the circumstances specified by the microcomputer. If the modem is receiving a packet and the scheduled time of a transmit occurs, the modem must determine if the transmit has been given a higher priority by the microcomputer. If so, the modem interrupts the receive, switches the RF unit into transmit, and retriggers the ECU activity with new control information.

When the radio is idling, which could be for some large number of slots at a time, the microcomputer needs some indication as to the quality of the settings it invokes in the modem. For example, threshold control requires a response of the number of false alarms occurring in a time slot. This is done by sending status information back to the microcomputer once each control time slot at the end of the time slot. The status is control-time-slot specific and only involves the modem and microcomputer.

When the radio is transmitting or receiving, packet-specific information is passed back to the microcomputer to be used for packet organization and analysis of the communication channel. Observations about the nature of a received packet are made at the RF unit, the modem, and the ECU. The RF unit at present observes the received power level, but with future enhancements would observe more. The modem observes such things as the packet time of arrival, the data-link header, and the multipath channel characteristics. The ECU observes the error statistics. The observations are compiled serially, each layer attaching its own to form a single set of observations. The observables flow from the RF unit to the modem to the ECU and finally to the microcomputer. The commands to the ECU actually come as observations specific to the packet upon which the ECU will operate.

Fig. 4 shows the activity during a typical received packet. The commands for control-slot *B* are delivered to the modem during slot *A* so they will be available in time. Likewise,



Fig. 4. Time frame for the radio receiving a packet. The commands, status, and observations (observ) are shown with their timing relative to the control time slots and the packet demodulation and error correction.

the commands for slot C are delivered during slot *B*. The status for each slot comes from the modem at the end of that slot to report on its activity. The observations frame the packet. The end of the packet, which occurs during slot C, still uses the parameters of code slot *B* in which the packet began. The sequential-decoding ECU could conceivably continue decoding long after the packet is finished demodulating in the modem. In that case, the tail end of the observations, which contain the error statistics, would be delayed enroute to the microcomputer.

The above discussion describes the relationship of the loosely coupled hardware-function layers of the radio. The level of complexity of the techniques used in this radio requires that such attention be paid to the design of the control and interface between the network-level hardware and the communication hardware, and among the communication hardware subunits.

III. SIGNAL PROCESSING

Comparison of Matched Filtering and Correlation

There are two receiver processes that are used under differing network conditions, creating two distinct operating modes of the radio. In general, the process of matched filtering the data bit provides a completely asynchronous method of demodulating the received signal. The process of correlation against an actively generated reference code [24] provides a synchronous method of demodulation. While matched filtering creates an output that is continuous in time representing all time relationships of the reference and the signal, correlation creates only one output sample, representing one value of the time relationship between reference and signal. As a consequence, a matched filter using convolvers requires simultaneous interaction with the entire reference waveform whereas the correlator does not. Lowering the data rate for greater signal-processing gain in a matched-filter receiver requires a longer interaction time which is highly technology-limited. For example, wide-band SAW devices have upper time-bandwidth product limits of about 2000 because the interaction time is typically limited to 20 μ s for 100-MHz devices [25], [26]. On the other hand, higher processing gain in the correlator is readily accomplished by integrating over a longer period of time [27].

A single correlator requires an accurate prior estimate of the arrival time of the signal. Alternatively, a bank of parallel correlators can be operated, each with a relative time shift of the waveforms incremented by the inverse of the bandwidth. Thus a less accurately estimated arrival time may be accommodated by framing the expected time window with the correlator bank. For initial detection, this correlator bank requires a total search time which equals the uncertainty in receiver timing multiplied by the processing gain, divided by the number of parallel correlators in the bank of detectors. In the matched filter, on the other hand, initial detection of a signal of unknown arrival time is immediate once the signal passes completely through the filter. Thus the matched filter exhibits no code-acquisition problem.

The radio described here uses a receiver which functions in the matched-filter mode when that provides sufficient processing gain; otherwise, it uses a parallel-correlator mode. To circumvent the correlator code-acquisition problem when using the very high processing-gain mode for initial detection, the timing uncertainty is reduced by prescheduling the arrival of packets. This prescheduled receive is treated as a special case in the local control by the microcomputer.

After synchronizing to the earliest detectable multipath

with a matched filter, the multipath echos that are used for RAKE demodulation appear at the output delayed in time. Alternatively, once detection has occurred for the correlator, the reference waveform and the correlator bank are retimed to align the correlator bank with the multipath processing window. Sequential readout of the correlator directly provides the multipath samples over a delay spread similar to that of the matched filter.

The correlator is also used in a special packet format where the modem asynchronously detects with the matched filter, synchronizes, and then the data portion is further processed with the correlator. The most accurate range measurements are performed in this way.

The Hybrid Processor

Fig. 5 shows a block diagram of the hybrid analog/digital signal processor in the modem. It consists of a programmable analog matched filter, an analog-to-binary interface, and a digital postprocessor. The matched filter uses two convolvers to provide continuous input-time coverage by alternately steering the reference waveforms between each convolver. The interface performs both coherent (heterodyne) and envelope detection, and creates several different 200-MHz-bandwidth binary-quantized input streams that are sent to the digital processor which selects from among these for a particular operating mode (Table I). The digital postprocessor consists of: the matched-filter code acquisition and RAKE demodulation circuits; two binary integrator channels; and hybrid-correlator code acquisition, RAKE demodulation, and TOA detection circuits. The various modes of operation tend to complement each other. For example, when the single channel of the binary integrator performs noncoherent TOA integration for the 90kbit/s data rate, part of the other channel is free to store the multipath profile used for the RAKE demodulation. In this manner, the wide range of operation is accomplished with surprisingly compact equipment.

The output of the SAW-based analog matched filter is approximately the impulse response of the communication channel, so the multipath signals will be easily discernable at the output as delayed correlation peaks. The input-time resolution of the output multipath profile is approximately



Fig. 5. The hybrid analog/digital signal processor located in the modem. The analog processing is on the left and the digital processing is on the right, adjoined by the analog-to-binary video interface.

10.8 ns, or the reciprocal of the spreading bandwidth of the waveform, 92.5 MHz. The binary RAKE [8], [13] noncoherently combines the multipath energy within a processing window to form a data decision. The accumulation of multipath energy can provide significant signal-processing gain. Although binary-digital RAKE is not as effective as maximal ratio combining, almost any process that adapts to the channel performs substantially better than a nonadaptive system (cf. [16, pp. 347, fig. 26]). The RAKE circuit described here is readily implemented in conjunction with SAW convolvers.

The operation of the binary integrator is described in detail in the digital processing section. Basically it accumulates successive windows of convolver output. By selecting the number of matched filter outputs used in a binary integration, the modem uses a data bit with selectable duration and thus adjusts data-bit energy. The hardware limit in this implementation is 1000 iterations, providing 30 dB of additional processing gain.

The three operational configurations that provide the selection of data rates are shown schematically in Fig. 6. The



Fig. 6. Operation of the hybrid processor for the various data rates available in the radio. The 1.45-Mbit/s and the 90-kbit/s rates use the matched filters and the binary RAKE. The lower rates use the analog matched filter and the binary integrator with binary RAKE.

top portion indicates the 1.45-Mbit/s mode which uses short convolvers. The RAKE demodulation occurs each data bit, accumulating the multipath energy. The 90-kbit/s mode uses the long convolvers and thus the convolver output impulses are drawn taller, indicating greater processing gain. The lower data rates (and also the other hybrid correlator applications) accumulate a binary quantized version of the convolver output to build up the processing gain with each iteration. The RAKE demodulation is used after the correlation.

The analog preprocessing and binary postprocessing make it possible to overcome the limitations encountered when using either technology alone. Analog signal processing components can handle very wide bandwidths but they provide only modest processing gain, e.g., 25–33 dB, and dynamic range, e.g., 30–45 dB [28]. Digital processing, on the other hand, supports large processing gains and dynamic ranges, but requires excessive power for wide-band applications. Analog preprocessing of non-Gaussian interference allows the digital postprocessing to occur with binary quantization of the input with minimal implementation loss [13], facilitating wide-band applications. When used together, these complementary technologies result in a very powerful hybrid of analog and digital processing.

Analog Processor

1) SAW Convolver: The schematic of the SAW convolver is shown in Fig. 7 [4], [29]. A signal and time-reversed ref-



Fig. 7. Simplified side view of a SAW convolver. The hornshaped waveguide creates an acoustic-beam compression resulting in sufficient power level to drive the piezoelectric crystal into nonlinearity thus forming the instantaneous product of the two input waves. The waveguide also acts as a collecting plate to perform the integration.

erence are counterpropagated along a piezoelectric delay line with a nonlinear interaction region. The resulting acoustic-wave interaction creates an instantaneous product of the waveforms which is summed along a metal plate to provide the convolution output. The processing gain of the convolver is the product of the interaction time of the convolver and bandwidth, referred to as the time-bandwidth product. The finest-resolution output of the fullbandwidth code generator is referred to as a chip. The timebandwidth product is also the number of chips per data bit, called the bandwidth-spreading factor. The waveform processed in the convolver is a 2048-chip section of a long m-sequence generated at 92.5 Mcps (chips per second), then minimum-shift-key (MSK) modulated onto a 300-MHz carrier [30]. The output is a function of the relative delay of the two waveforms, and since the two waveforms are counterpropagating the relative velocity is increased by a factor of two, resulting in a bandwidth doubling at the convolver output. For the 92.5-Mcps input rate, the output digital-signal-processing circuits must therefore be clocked at 185 MHz.

2) Processing Gain: The processing gain of the convolver is illustrated in Fig. 8. On the left side is the input spectrum and on the right side is the time-domain output. For excellent signal-to-noise ratio at the convolver input, the output shows the detectable signal is only disturbed by code sidelobes. In the middle two photographs, the noise is raised to the input signal level and the output peak is approximately the same as the previous photograph set. In the third set, the input noise is raised another 20 dB and the convolver output peak is approximately 10 dB above the noise, which is sufficient for demodulation.

3) Modulation: Data modulation on the spread-spectrum signal is implemented with differential phase tran-



Fig. 8. The performance of a convolver in random noise. The input spectrum is on the left and the output time-domain signal is on the right. The top set of photos shows good signal-to-noise ratio. The middle set shows approximately 0-dB input signal-to-noise ratio, and the bottom set shows approximately –20-dB input signal-to-noise ratio.

sitions. Two convolvers, formed with a segmented waveguide on one crystal, can be used to directly demodulate a differential phase-shift-keyed (DPSK) signal (Fig. 9) [8], [31]. The outputs of the two $11-\mu$ s convolver segments are combined coherently in an RF hybrid. When data create a phase transition between 2 bits, the convolution spike comes out of the difference port of the hybrid and only noise comes out of the sum port. If no phase transition is present, the output comes out of the sum port.

The spreading code is composed of serially aligned sections of a much longer sequence which is generated from a 3-byte start vector (PN seed). A new start vector is delivered to the modem from the microcomputer over the com-



Fig. 9. Simplified DPSK convolver.

mand interface each 10 ms. The 100-MHz code is at present generated in ECL technology; however, most of these circuits could soon be replaced by a highly parallel NMOS chip which has been fabricated at the DARPA MOSIS silicon foundry [32]. The MSK modulation is generated by PSK modulation of weighted quadrature channels [33]. For the nominal 90-kbit/s data rate of the radio, 1024 chips of the PN sequence are transmitted per data bit. Two bits worth of energy are used in each DPSK demodulation. The 1.45-Mbit/s high data rate is implemented using shorter convolvers with 64-chips-per-bit binary orthogonal keying (BOK), giving almost 18 dB of signal-processing gain [34]. The ability of the convolver reference to change at the full signal bandwidth, and hence to change the code on each bit, is very important at the high data rate to suppress intersymbol interference by a factor equal to the processing gain [16]. The changing codes also offer additional privacy. An RF switching matrix allows the multiplexing of the input MSK waveforms and convolver outputs.

4) Synchronization: The propagating reference in the convolver allows continuously changing codes to be used; however, it requires that two convolvers be used to provide continuous time coverage. The asynchronous detection of an incoming signal uses both of these convolvers, staggered in time by one 22-µs convolver length [8], [35], [36]. To obtain the full processing gain over all arrival times of the signal, a reference that is twice as long as the convolver interaction region is used. The result is two full convolvers worth of energy for matched-filter detection with the minor sacrifice of 22 μ s of extra signal that must be transmitted. After this detection, the codes are made the same length as the convolver and the receiver realigns its code to the received code, thus synchronizing. The multipath processing window is placed appropriately to obtain the maximum processing gain available for demodulation.

The beginning of a typical packet is illustrated in Fig. 10.



Fig. 10. A typical received packet at the 90-kbit/s data rate. The top photograph is the output of the sum port of the DPSK demodulator and the bottom trace is the output of the difference port.

At the start of each packet, a preamble is transmitted which contains no data transitions; thus the output occurs on the sum port. After the preamble, the packet header is demodulated, with data appearing in either port. After the header, the text is demodulated. The portion of text in the figure is alternating groups of four binary ones and zeros. The text would continue for the length specified in the header.

Digital Processing

1) CFAR Detection: The receiver detection threshold is adaptively corrected to maintain a constant rate of false signal detections in spite of fluctuating interference. The network control algorithms would set the desired false alarm rate on a slower time scale. Typical false alarm rates range between one per second and one per hundred seconds. Threshold control is critical, as excessive false alarms would create excessive time for the receiver to be blanked, and a threshold resulting in too few false alarms would allow too many missed signal detections and reduce the radius of connectivity the receiver has within the network.

During the packet preamble, correlation spikes appear at the sum port of the convolver, and both the sum and the difference port will have equal-power, uncorrelated noise and code sidelobes. Linear envelope detection and a lowpass filter on the difference port thus provides a simple implementation of a CFAR threshold (Fig. 11). Code sidelobes



Fig. 11. Multipath-resistant CFAR detection. The DPSK convolver difference-port output is used as a noise reference.

from multipath signals add within a bit creating interpath interference [16]. The equality of sidelobe power between the two ports still holds, creating a multipath resistant CFAR circuit. The CFAR circuit drives the analog input of a multiplying D/A converter (MDAC) which generates the detection threshold. The digital value in the MDAC scales the detection threshold and is set by the microcomputer through the interface and control logic.

2) Digital RAKE: It has been observed that the envelope decorrelation due to multipath fading [16], [37] occurs over a time scale substantially greater than 10 ms for ground vehicle speeds [38]. Thus it is adequate to sample and store the multipath profile only once per packet for packets at 1.45 Mbits/s and 90 kbits/s. During the packet preamble the output of the CFAR detector is sampled and stored in shift registers whose clock timing defines the processing window (Fig. 12(a)). The multipath profile is thus stored for the 90-kbit/s and the 1.45-Mbit/s data rates. The preamble always uses 22-µs signaling in the long convolver, thus acting to sound out the channel for the high data rate with excess signal-to-noise ratio and without the burden of intersymbol interference to disturb the profile.

The digital RAKE uses a counter running at 185 MHz to sample the full multipath resolution. The stored profile is recirculated each data bit in order to enable the RAKE counter to sample, while the running DPSK decision is applied to the count-up/count-down input. Shown in Fig. 12(b) are the RAKE circuit and digital waveforms for the data and the multipath. Only when the profile indicates the presence



Fig. 12. RAKE demodulation. (a) Multipath-profile storage during the message preamble. (b) Demodulation using the stored profile as it recirculates. CE is the enable to the counter, U/D is the count-up count-down input to the counter, and MR is the reset which is asserted after each data bit is read out.

of a path (a logic one in the figure) is the DPSK input allowed to vote, thus eliminating the noise-only parts of the DPSK stream. The most significant bit of the count yields the result of the majority vote process providing the resulting data decision [8], [13]. This method of accumulating multipath energy is actually correlation against the multipath profile.

3) Correlation: The operation of the binary integrator is shown in Fig. 13. The multipath processing window of the convolver is of high bandwidth and short duration, lending itself to low-bandwidth, long-duration postprocessing. The sampled and binary-quantized output is stored in parallel shift registers at high speed during the active output window and is read out at a fraction of the speed into an accumulating memory between windows [6]. We show one of the two binary integrators which comprise a fast-in/slowout (FI/SO) storage and an accumulating memory. The accumulating memory is a bank of shift registers that recirculate through an arithmetic logic unit. An exclusive-or function is used to remove data transitions and for chopper stabilization of the integrator.

The binary quantization simplifies the integrator circuitry. The FI/SO storage registers are 4 TTL chips fed by a few ECL chips. The accumulating memory uses 12 TTL chips. In total, the two channels of binary integration including clocking circuits occupy approximately 15 in² and most of that is reused for the other modes of the radio. As a more compact alternative, a prototype NMOS binary integrator chip was made at the DARPA MOSIS silicon foundry [32].

A variety of options are available with the binary integration as determined by the microcomputer and receivedpacket header. Coherent integration, noncoherent integration, and double-threshold detection are three tech-



Fig. 13. The binary integration technique for SAW-convolver outputs. The short-duration outputs are stored in the FI/SO buffer and then processed in the accumulating memory.

niques that are used; we will only describe the coherent mode of operation in this paper. Detailed descriptions of the other operating modes and the multipath processing may be found elsewhere [6], [7].

Coherent integration is only used when the Doppler shift due to motion between the transmitter and receiver is small. If there is substantial Doppler shift, the noncoherent binary integration mode must be used at a sacrifice in integration gain. The sacrifice is illustrated in Fig. 14 which compares coherent and noncoherent integration for 1000 accumulations of the convolver output. The input energy per bit divided by the noise power density (E_b/N_0) at the input to the binary integrator is plotted against the output signal-tonoise ratio. Significant benefit is obtained from coherent integration at input E_b/N_0 values less than -3 dB.

The coherent postprocessor is shown in Fig. 15. The RF waveform out of the convolver is heterodyned with in-phase

and quadrature carriers to obtain the bipolar baseband signals. These are then compared to zero and integrated separately in the two channels of the binary integrator. The results are squared and summed, and then this magnitudesquared value is compared to a threshold for detection. The detections are used for preamble detection of a scheduled reception, and are stored and updated as multipath for demodulation. Data may be demodulated using this coherent integration by performing DPSK comparisons between each integrated data bit. In this case, all the matched-filter outputs integrated into a bit have no phase transitions, but an adjacent bit may have a 180° inversion on the carrier phase on all convolver outputs. The signs of the bit accumulations are compared on a sample-bin-by-sample-bin basis. RAKE demodulation is performed using the detection profile obtained from the sum-of-squares process. For these lower data rates, the multipath must be updated each data bit since



Fig. 14. Comparison of coherent and noncoherent binary integration for 1000 integration cycles.



Fig. 15. Coherent correlation for DPSK data demodulation. DPSK demodulation is performed between integration periods, on a correlation sample by correlation-sample basis, and the results are then accumulated in a RAKE circuit. The l < > Q signal tells the DPSK estimator which channel contains the largest magnitude for each sample.

the data bit lengths could be over 20 ms (44 bits/s). For each DPSK decision sample that is accumulated in the RAKE processor, the result of a correlation sample of the current correlation must be compared to the result of the corresponding sample of the previous correlation. The results of these individual comparisons are accumulated in the RAKE for each data bit over a multipath processing window. In doing the comparison, an approximation can be used that only requires the sign bit of the result of the previous correlation and not the full value, thus alleviating the storage requirements.

When using the hybrid correlator for demodulation, the RAKE processing window covers $2.76 \,\mu$ s of convolver input time representing 256 parallel correlations. The binary-integrator RAKE runs at less than 25 MHz due to the FI/SO buffering, although it is otherwise like the higher rate RAKE circuits. Because initial detection of a packet with the binary integrator is a correlation process, a prior estimate must be made of where to place the processing window; however, the correlation search time that is normally encountered is reduced by the number of resolution elements in the window or 256.

IV. ENHANCEMENTS AND FUTURE DIRECTIONS

Device Technologies

Although the demonstration radio described above is based on 100-MHz bandwidth devices, the techniques and architecture developed are generally applicable to more modest bandwidth signal processing. Lower bandwidth processing, although less robust, can be made much smaller, lower power, and lower cost. CCD matched filters, replacing the SAW matched filters combined with high levels of IC integration that could be used at the modest bandwidths might lower the cost and size of a packet radio with this architecture by more than an order of magnitude while lowering the spread-spectrum data-link performance by only a factor of four.

The IC simulation and processing advances made to support digital technology have also worked in favor of CCDs to solve the major problems holding back high-speed applications. A device that performs a complete two-channel analog-binary matched-filter function with 25-MHz bandwidth and processing gain in excess of 20 dB has been made on a small, self-contained chip which consumes less than 1 W [17]. Furthermore, near-term projections have been made for a device fabricated in 2-µm CMOS technology that will have 50-MHz bandwidth and 30-dB processing gain. Long-term projections are for bandwidths into the range of several hundred megahertz. Combining CCD technology with dedicated digital VLSI postprocessing chips will create even more powerful hybrid analog/digital signal processors for packet radios. In fact, the CCD has the advantage that digital postprocessing circuitry can be integrated on the same monolithic chip.

A more exploratory yet potentially high-performance technology is the acoustic-charge-transport (ACT) device [39]. ACT devices offer CCD-like sampling using SAW for charge transport. Preliminary devices have demonstrated 200-MHz signal bandwidth. Long-term projections are for bandwidths of over a gigahertz and time-bandwidth products of several thousand.

Front-End Processing

The linear correlator techniques allow a sacrifice of data rate to combat intense interference; however, it may not always be possible to support data-link requirements with these lower data rates. The combination of data traffic and network control traffic required during network transient periods can create insurmountable traffic requirements to maintain a node in the network. In many cases, nonlinear signal processing techniques can be added to provide interference suppression without the expense of lower data rates. For the ultimate in processing, these nonlinear techniques can be used with the lower data rates.

Typically, a broad-band received signal is contaminated by a number of in-band interference signals. The matchedfilter receiver can only discriminate against interference to the extent of its processing gain. Often, either a single interference signal or the average sum of the interference is so large that it cannot be processed using matched filtering techniques. In most of these cases, however, the interference is large enough to be estimated and adaptively canceled before entering the matched filter. The cancellation need only bring the total interference to within the processing range of the receiver. If the matched filter has 30dB processing gain, then the total interference energy should be no more than 15-20 dB greater than the total signal energy to ensure sufficient output signal-to-noise ratio for reliable decisions. In the case of narrow-band interference, it is possible to match these nonlinear cancellation circuits to the interference. For wide-band interference, however, only a correlation-type receiver matched to the signal can identify the signal energy. Thus the job of the front-end circuits becomes one of isolating the wide-band signals and normalizing them to equal powers. This would allow the matched filter in the modem to do its job of determining which is the desired signal and which is the interference.

Circuits dedicated to the removal of a single large narrowband interferer can be used immediately following downconversion to prevent receiver saturation [40]. A phaselocked loop is used to derive a clean estimate of the interference which dominates the incoming signal. The estimate is then subtracted from the original input. A feedback loop is used to correct the amplitude and phase of the subtracted estimate, resulting in over 40 dB of cancellation.

Fourier-transform-based excisor techniques have been reported [41] that can be used to eliminate multiple moderate-level narrow-band interferers. When implemented with SAW reflective-array-compressor (RAC) chirp filters, one can create an adaptive-filtering structure for wide-band spread-spectrum transmission [42]. A signal is first chirp Fourier-transformed so that its frequency spectrum is mapped into a time function. This signal is then time-gated to excise narrow-band spectral components. The gated spectrum is then inverse-transformed to create a filtered version of the signal. The process operates in real time and delays the signal by no more than tens of microseconds. Typical design parameters permit the use of dozens of excision notches narrower than 0.5 MHz over about a 100-MHz band, with as much as 20 dB of narrow-band suppression in each, and greater than 30 dB of dynamic range (relative to the PN signal at the system output). Substantial benefit can be gained before a significant portion of the desired signal energy is notched out of the spectrum along with the interference.

Another problem which must be overcome in the operation of a wide-band PN radio network is the potential for the signal from a near (strong) wide-band radio to overwhelm that from a distant (weak) one by more than the processing gain. This has been referred to as the near/far problem. Circuits can be made to separate the two signals.

However, due to the similarities of the two signals, only in contrived circumstances can these circuits determine if the near/far problem is actually occurring. Thus autonomous canceling is generally not appropriate. Instead, once the signals are separated they should be normalized and recombined with commensurate powers. The result is passed to the matched filter which can readily process away the interferer. A large wide-band signal (L) may be isolated from a small wide-band signal (S) in several ways. One technique takes advantage of the well-known small-signal-suppression effect of a bandpass limiter [43], [44]. When a small signal and a uniform-amplitude high-level signal are simultaneously passed through a bandpass limiter, the small signal is suppressed in amplitude by 6 dB relative to the large signal. Because the phase through the bandpass limiter is preserved, the resulting signal (proportional to L + 1/2 S) can be amplified and subtracted from the original signal, thus canceling the large uniform-amplitude component (L) and retaining a fraction of the small component (1/2 S). The isolated small signal may now be normalized, with an AGC, to the level of the original signal ($\cong L$) which is dominated by the large interferer. The two signals of equal power are added together and the processing gain of the matched filter is then sufficient to discriminate between the signal and interference. Other techniques have been postulated for isolating two independent signals of differing amplitudes that occupy the same band [45].

An issue regarding these circuits which must be addressed is whether they should react autonomously to the input or if there should be some direction from the network. There are cases where the type of interference that the circuit is designed to operate on may not be present and the circuit, left in operation, would incur an implementation loss. Also, care must be taken when using the circuits simultaneously. Distortion effects and dynamic range considerations result in preferred orderings of the application of the cancelers. If the network algorithms control the cancelers, they must get inputs regarding the channel behavior. Channel conditions can readily be inferred from the spectrum in the chirp transformer, the phase-lock-loop error voltage in the narrow-band canceler, the AGC error voltage, and the difference in input and output power of the wide-band cancellation circuits.

Incorporating Data-Link Control

With the signal-processing capabilities of this radio comes an increase in the control complexity; this poses a challenge for developing network software. The network control is complicated by the large number of parameters that can be adjusted in response to a large set of inputs, resulting in a formidable if not intractible control problem. A reasonable approach would be to loosely couple the data-link control and the network control. Loose coupling allows the network and data-link problems to be solved separately under coarse constraints from each other. If each solution were optimized nearly independently, then the combination is generally less than optimum but possibly still quite good.

The proposed approach is predicated on the development of a high-level model of the data link and a data-link control process (DLCP). These would necessarily be provided by those familiar with the data-link technology. The DLCP would be a software process which exists conceptually as a layer between the network and the data link. The process would be queried by the network software for possible actions that could be taken in the face of link degradation and changing network requirements. It would perform the computations based on packet activity and channel measurements and then evaluate and report back to the network the tradeoffs for deciding on how best to allocate the signal-processing assets. The signal-processing circuits in the modem, the error-correction circuits, the AGC in the RF unit, and any front-end adaptive cancellation circuits would make available a fair number of local channel parameters which could be circulated throughout the network for distributed control. The DLCP would make available to the network level a high-level interpretation of these parameters and suggested courses of action. The DLCP also would provide the network software with the ramifications of the suggested course of action. The details of the signalprocessing implementation end up being buried in the design of the DLCP. Thus the network designers do not need to understand the details of the signal-processing tradeoffs.

For example, the network-control software would simply ask for more privacy for a mobile node, rather than specifically requesting a matched-filter synchronization and a 350-bits/s text data rate with noncoherent binary processing. Since any high-level request from the network will have a number of possible solutions at the data link, the network must choose from a list of solutions with corresponding ramifications in an attempt to optimize network performance. The ramifications are, in turn, inputs in the ongoing network algorithms. When provided with a high-level model, an interface, and a limited set of possible responses and ramifications, the programming effort becomes quite tractable.

V. CONCLUSIONS

Major advances have been made in both the architecture and the signal processing for packet radio. Wide-band highprocessing-gain programmable matched filters and versatile digital postprocessing have been combined to create a multifunction signal processor for spread-spectrum communications and ranging. A systematic interface in a layered design structure has been adhered to for high-level control of the advanced processor. Further advances are on the way and it is necessary for the network-level designers to remain in close relationship with the signal-processing designers to derive full benefit from these advances.

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John H. Cafarella (Member, IEEE) received the Sc.D. degree from the Massachusetts Institute of Technology, Cambridge, in 1975. His graduate studies concentrated in electromagnetic and acoustic fields, solidstate physics, and microwave circuits. His thesis research was in surface-acousticwave signal-processing devices, particularly convolvers and memory correlators.

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Gerard T. Flynn (Member, IEEE) received the B.S. degree in physics electronics from LaSalle College, Philadelphia, PA, in 1963. He is currently a staff member at Massachusetts Institute of Technology, Lincoln Laboratory, Lexington, MA, engaged in the design of airborne radar systems. From 1980 to 1986 he worked in the Analog Device Technology Group at Lincoln Laboratory where he was responsible for the design of the RF and IF portions of the spread-spec-

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gorithms, architectures, and circuits for the application of advanced analog signal processing devices. This work included design and analysis for the spread-spectrum radio described in this paper and the development of adaptive clutter-suppression techniques using nonrepeating pseudonoise radar waveforms. He is currently a graduate student at Princeton University, Princeton, NJ, where his interests are in the areas of digital signal processing and statistical image modeling.



Fig. 1. Photograph of the radio hardware. The *L*-band RF unit is on the right. The other three units reside in the chassis on the left.



Fig. 8. The performance of a convolver in random noise. The input spectrum is on the left and the output time-domain signal is on the right. The top set of photos shows good signal-to-noise ratio. The middle set shows approximately 0-dB input signal-to-noise ratio, and the bottom set shows approximately –20-dB input signal-to-noise ratio.



Fig. 10. A typical received packet at the 90-kbit/s data rate. The top photograph is the output of the sum port of the DPSK demodulator and the bottom trace is the output of the difference port.